

In the Drawings

The attached sheet of drawings includes a change to FIG. 6. The replacement sheet 3/4 includes FIGS. 3 and 6. In FIG. 6 the comparator has been changed to "604."

Attachment: 1 Annotated Sheet showing changes
1 Replacement Sheet

Remarks

This is a complete response to the Office Action mailed July 28, 2005. The amendments and remarks are proper, do not add new matter, are not narrowing in view of a rejection over a cited reference, and place all claims in condition for allowance.

Objection to Claims

Claim 2 was objected to for two informalities.

First, the Examiner suggested that “a numerical phase difference value” should be “the numerical phase difference value.” Applicant has amended claim 2 accordingly to obviate the objection. Withdrawal of the objection is respectfully requested.

Second, the Examiner suggested that “wherein the encoding circuitry converts the values stored in the parallel latch into a numerical phase difference value” is redundant to the claimed features in claim 7. Applicant respectfully traverses this objection. Claim 7 recites the following:

a phase detecting stage that generates a result...

wherein the encoding circuitry converts a result of the phase detecting stage into a numerical phase difference value and outputs the transition location signal.

(excerpt of claim 7, emphasis added)

Claim 2 further describes the “phase detecting stage” as having a “parallel latch,” and further provides that the encoding circuitry “converts the values stored in the parallel latch into the numerical phase difference value.”

Accordingly, the language of claim 2 actually provides additional limitations to the recited features of claim 7, and is therefore not merely redundant language.

Reconsideration and withdrawal of this objection to claim 2 are respectfully requested.

Rejection Under Section 112 Second Paragraph

Claims 1, 8, and 9 were curiously again rejected as being non-enabling for omitting essential elements, citing MPEP 2172.01. However, applicant reiterates that MPEP 2172.01 provides that a claim can be rejected under Section 112 paragraph 1 for omitting essential elements, or can be rejected under Section 112 paragraph 2 for failure to interrelate essential elements. Here, the Examiner has based a Section 112 paragraph 2 rejection on omitting essential elements, for which there is no basis in the law or in the MPEP section on which the Examiner relies.

Applicant can only respond to this rejection to the extent it is understood, because the rejection does not comport with the Examiner's obligation to provide a complete examination with respect to compliance of the application with statutes and rules. (37 CFR 1.104(a)) Regardless of whether the Examiner sets out a paragraph 1 or 2 rejection under Section 112, such rejection must be substantiated by an evidentiary showing of what the essential matter is:

A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may be rejected under 35 U.S.C. 112, first paragraph, as not enabling...In addition, a claim which fails to interrelate essential elements of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. 112, second paragraph, for failure to point out and distinctly claim the invention.
(MPEP 2172.01, emphasis added)

Applicant reiterates that there is no essential matter that is either omitted or inadequately interrelated such that a Section 112 rejection is warranted. The Examiner has

not substantiated a traversal of Applicant's previous rebuttal in that regard.

In rejecting these claims the Examiner further stated: "claim 1 is simply a preamble, and there is no means in claim 1 to perform the recited function. See MPEP 2111.02, 2111.03, and 2114." (Office Action of 7/28/2005, pg. 3, emphasis added) However, none of the cited portions of the MPEP substantiate the Examiner's assertion that claim 1 is in improper form. That is, MPEP 2111.02 describes the limiting effects of a preamble; MPEP 2111.03 describes the meaning of transitional terms; and MPEP 2114 describes that functional limitations must be distinguishable by structural differences in relation to cited references.

Applicant reiterates that claim 1 is not in means-plus-function form. (see Amendment filed 2/15/2005, pg. 7; Appeal Brief filed 5/16/2005, ppg. 3-4) First, there is no claim language triggering a means-plus-function construction. Furthermore, an apparatus claim drawn to a circuit and coupled with a description of the circuit's operation connotes sufficient structure to persons of ordinary skill such that Section 112 para. 6 presumptively does not apply. *Linear Technology Corp. v. Impala Linear Corp.* 72 USPQ2d 1065 (Fed. Cir. 2004); *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003).

Accordingly, this rejection is invalid for failure to comport with the Examiner's obligations to make a complete examination with respect to form and patentability of the invention as claimed. Withdrawal of the rejection is respectfully requested.

Rejection Under Section 102(e)

Claims 1-3, 7, 10-12, 16, 17, 20-22, 25, and 26 were rejected as being anticipated by Staszewski '693. Applicant respectfully traverses this rejection.

Claim 1

Applicant reiterates that Staszewski '693 cannot sustain a Section 102 rejection of claim 1 because it fails to identically disclose all the recited features of the present embodiments, including at least the following:

An apparatus comprising a phase/frequency comparator circuit that is configured to generate a phase error responsive to a transition location signal.
(claim 1, emphasis added)

Applicant rebutted the Examiner's anticipatory rejection of claim 1 over Staszewski '693 on the basis that it fails to identically disclose the *transition location signal* (see Applicant's Response of 2/15/2005, ppg. 10-11, Appeal Brief filed 5/16/2005, pg. 8). The Examiner now traverses Applicant's rebuttal first by urging that Staszewski '693 inherently discloses the transition location signal, and second by wholly ignoring explicitly recited claim features. Particularly, the Examiner cites the following as the basis for the anticipatory rejection:

With regard to claim 1, Staszewski et al. discloses in Figs. 1-8 a phase/frequency comparator (804) that inherently generates a phase error responsive to a transition location signal...Furthermore, the limitation "generates a phase error responsive to a transition location signal" is purely a result function of the phase/frequency comparator and thus has not been given patentable weight....
(Office Action of 7/28/2005, pg. 4, emphasis added)

The Examiner's attempted traversal of Applicant's rebuttal is ineffective because it is reversible error.

Inherency

As for the Examiner's inherency argument, the claim language plainly means that the signal of concern, the *transition location signal*, conveys information about the location of the transient transition signal. This meaning is consistent with the term's explicit definition and usage in the specification:

N-bit parallel latch 302 latches in the outputs of N-bit tapped delay line 300 when reference clock signal 303 transitions (either from low to high or high to low, depending on the latch design). The output of N-bit parallel latch 302 is thus a snapshot of the progress of input signal 301 through N-bit tapped delay line 300 over one cycle of reference clock signal 303. This snapshot is fed into N-bit edge detect circuit 304, which is described in more detail in FIG. 4. N-bit edge detect circuit 304 outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch 302. This signal bit may be referred to as a transition location signal.

(specification pg. 7 lines 1-10, emphasis added)

The Examiner acknowledges by the allowable subject matter the distinguishable structural differences in the present embodiments, but curiously fails to acknowledge the novel functional capabilities associated with the structural differences. Particularly, the *transition location signal* directly indicates the state of occurrence of the transition signal with respect to the most recent clock reference cycle. For example, referring to FIG. 3 and the description thereof, in some embodiments the N-bit tapped delay line 300 initializes at the beginning of each clock reference 301 cycle. The snapshot taken by the N-bit parallel latch directly indicates the progress (location) of the clock reference cycle 301 through the N-bit tapped delay line 300 precisely at the occurrence of the reference transition signal

303. Accordingly, the present embodiments indicate the location of the transient transition signal by observing it in relation to a known reference point; that is, for example, by observing it in relation to the beginning of the most recent clock reference cycle.

Contrarily, Staszewski '693 is wholly silent regarding a signal conveying information about the location of a transient transition signal, but rather discloses a signal conveying information about the relative timing between the reference transition signal 110 and the clock 114:

FIG. 6 is a timing diagram 600 associated with the time-to-digital converter 500 shown in FIG. 5. During a positive transition 602 of the reference oscillator FREF 110, the plurality of latch/registers 504 are accessed to obtain a snapshot 604 of the delayed replicas of the dVCO clock CDV 114 relative to the rising edge of the reference oscillator FREF 110. The snapshot 604 can be seen to express the time difference as a digital word.
(Staszewski '693, col. 8 lines 39-46, emphasis added)

In Staszewski '693 the transition signal is observed randomly; in other words, without relating its occurrence to any previously defined reference point. That is, Staszewski '693 replicates a plurality of clock reference cycles ($D(0) - D(9)$) between each clock signal 114. The TDC_RISE (or TDC_FALL) signal from the time-to-digital converter 500 of Staszewski '693 merely indicates which of the replicated reference cycles reflects a transition change at the time of the snapshot. The digital word ($Q(0:9)$) in Staszewski '693 obtained by the snapshot is subsequently synthesized in order to determine Δt_r (or Δt_f), the result then being normalized in order to determine the timing error or phase difference. (see, for example, Staszewski '693 col. 8 lines 46-55)

"To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it

would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) Staszewski '693 clearly discloses a time-to-digital converter that outputs a signal reflecting a relative timing difference. The skilled artisan recognizes that without definition in relation to when the timing began, or of a timing reference point, the output signal of Staszewski '693's time-to-digital converter is inherently incapable of conveying information as to the location of the transient transition signal as in the present embodiments as claimed.

The skilled artisan will also recognize that Staszewski '693 suffers from the same shortcomings as the counter-based designs that are resolved by the embodiments of the present invention. (see, for example, specification pg. 4 lines 15-27). That is, because Staszewski '693 relies on progressively replicating the clock references, it becomes impractical for use with high-frequency reference transition signals where the clock reference signal must be orders of magnitude higher in frequency for an acceptable accuracy.

The Examiner's claim construction is unreasonable because it ignores both plain meaning and the explicit definition in the specification of the claim term *transition location signal*. *In re Morris*, 43 USPQ2d 1753 (Fed. Cir. 1997). Staszewski '693 cannot sustain a Section 102 rejection for failure to identically disclose all the features of the present embodiments as claimed.

Functional Limitation

The Examiner furthermore attempts to traverse Applicant's rebuttal by ignoring explicitly recited claim language; this is reversible error. There simply is no basis in the law for outright ignoring explicitly recited claim elements in construing claims. By giving patentable weight to only a portion of the recited claim elements, the examination resulting in the final rejection is incomplete with regard to the Examiner's obligation to determine the patentability of the invention as claimed. 37 CFR 1.104(a).

The Examiner's claim construction is erroneous because it wholly ignored explicitly recited functional features of the present embodiments. Particularly, the present embodiments as claimed cover a circuit that is *configured to generate a phase error responsive to a transition location signal*, which is distinguishable over the timing difference signal of the time-to-digital converter circuit of Staszewski '693.

Contrary to the Examiner's apparent misunderstanding of claim construction, there is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. *In re Swinehart*, 169 USPQ 226 (CCPA 1971). "A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in association with an element...to define a particular capability or purpose that is served by the recited element...." MPEP 2173.05(g)(emphasis added), citing *Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc.*, 72 USPQ2d 1001, 1006-08 (Fed. Cir. 2004)

Here, the skilled artisan readily recognizes that the functional limitation *configured to generate a phase error responsive to a transition location signal* defines a particular

capability to directly determine the state of the transition signal in relation to a known reference point, as opposed to observing a relative timing difference and subsequently calculating the phase difference.

When properly construed, a skilled artisan readily recognizes that the claimed feature *configured to generate a phase error responsive to a transition location signal* defines novelty in the capability of the phase/frequency comparator, resulting from bona-fide structural differences between the claimed embodiments and the cited reference. Because the Examiner improperly ignored explicitly recited claim elements, the examination resulting in the final rejection of claim 1 is incomplete with regard to the Examiner's obligation to determine patentability of the invention as claimed. 37 CFR 1.104(a)

Conclusion

Thus, in conclusion as to the Section 102 rejection of claim 1 over Staszewski '693, the Examiner's attempted traversal of Applicant's rebuttal is ineffective as reversible error. Particularly, the Examiner has failed to substantiate that Staszewski '693 inherently discloses the *transition location signal*, and there is no basis in the law for the Examiner not affording the feature patentable weight for being a functional limitation. Reconsideration and withdrawal of the present rejection of claim 1 and the claims depending therefrom are respectfully requested.

Claim 10

Staszewski '693 cannot sustain a Section 102 rejection of claim 10 because it fails to identically disclose all the recited features of the present embodiments, including at least the following:

*A phase locked loop comprising...wherein the
phase/frequency comparator includes...encoding circuitry
coupled to the phase detecting stage....
(claim 10, emphasis added)*

The skilled artisan recognizes that an *encoding circuitry* generally changes the format of the data without changing the value of the data substantively or quantitatively. This distinguishes *encoding circuitry* from other algorithmic circuit processes performing mathematical operations on the data such as by addition and division and the like. This meaning is consistent with the term's usage in the specification:

Weighted encoder 306 converts the output of N-bit edge-detect circuit 304 into a numerical phase difference value that reflects the phase difference between input signal 301 and reference signal 303.

(specification pg. 7 lines 11-13, emphasis added)

The Examiner read the period normalization circuit of FIG. 2 as anticipating the *encoding circuitry* of the present embodiments as claimed. However, the period normalization circuitry plainly is an algorithmic operation performing mathematical operations on the data to quantitatively change its value:

ϵt_r has to be normalized by dividing it by the clock period,
in order to properly combine it with the integer phase
detector output, θ_d .

(Staszewski /693, col. 7 lines 21-24, emphasis added)

Again, the Examiner by the indication of allowable subject matter acknowledges the structural distinction of the weighted encoder 306 of the present embodiments, but curiously seems to ignore that distinction in construing the language of claim 10. If, as the Examiner urges, a mathematical operation can be construed to read on an *encoding circuitry* then the ultimate conclusion is that any circuit would have to be reasonably considered an *encoding circuitry*. Such would be an absurd conclusion to the skilled

artisan, and would require ignoring an explicit term appearing in the claim. Rather, the Examiner's claim construction is unreasonable because it ignores both plain meaning and the explicit definition in the specification of the claim term *encoding circuitry*. *In re Morris.*

Accordingly, Staszewski '693 cannot sustain a Section 102 rejection for failure to identically disclose all the features of the present embodiments as claimed. Reconsideration and withdrawal of the present rejection of claim 10 and the claims depending therefrom are respectfully requested.

Claim 20

Applicant reiterates that Staszewski '693 cannot sustain a Section 102 rejection of claim 20 because it fails to identically disclose all the recited features of the present embodiments, including at least the following:

A method comprising...mapping the snapshot to a numerical phase difference value that is generated responsive to a signal that corresponds to a transition location of the first signal....
(claim 10, emphasis added)

Applicant rebutted the Examiner's anticipatory rejection of claim 20 over Staszewski '693 on the basis that it fails to identically disclose the *signal that corresponds to a transition location of the first signal* (see Applicant's Response of 2/15/2005, ppg. 10-11, Appeal Brief filed 5/16/2005, pg. 8). The Examiner now repeats the rejection with no more substantive traversal than to identify TDC_RISE, TDC_FALL as reading on the *signal that corresponds to a transition location of the first signal*. (Office Action of 7/28/2005, ppg. 5-6)

For the reasons discussed above (and summarized here for brevity sake), Staszewski '693 is wholly silent regarding a signal conveying information about the location of a transient transition signal, but rather discloses a signal conveying information about the relative timing between the reference transition signal 110 and the clock 114. The TDC_RISE (or TDC_FALL) signal from the time-to-digital converter 500 of Staszewski '693 merely indicates which of the replicated reference cycles reflects a transition change at the time of the snapshot. The digital word (Q(0:9)) in Staszewski '693 obtained by the snapshot is subsequently synthesized in order to determine Δt_r (or Δt_f), the result then being normalized in order to determine the timing error or phase difference. (see, for example, Staszewski '693 col. 8 lines 46-55) Staszewski '693 clearly discloses a time-to-digital converter that outputs a signal reflecting a relative timing difference. The skilled artisan recognizes that without definition in relation to when the timing began, or of a timing reference point, the output signal of Staszewski '693's time-to-digital converter is inherently incapable of conveying information as to the location of the transient transition signal as in the present embodiments as claimed.

As above, the skilled artisan will also recognize that Staszewski '693 suffers from the same shortcomings as the counter-based designs that are resolved by the embodiments of the present invention. (see, for example, specification pg. 4 lines 15-27). That is, because Staszewski '693 relies on progressively replicating the clock references, it can become impractical for use with high-frequency reference transition signals where the clock reference signal must be orders of magnitude higher in frequency for an acceptable accuracy.

The Examiner's claim construction is unreasonable because it ignores both plain meaning and the explicit definition in the specification of the claim term *signal that corresponds to a transition location of the first signal*. *In re Morris*, 43 USPQ2d 1753 (Fed. Cir. 1997). Staszewski '693 cannot sustain a Section 102 rejection for failure to identically disclose all the features of the present embodiments as claimed. Reconsideration and withdrawal of the present rejection of claim 20 and the claims depending therefrom are respectfully requested.

Rejection Under Section 103

8, 9, 18, and 19 were rejected as being unpatentable over Staszewski '693 alone or in view of Brachmann '154. This rejection is respectfully traversed in that these claims are allowable as depending from an allowable independent claim, for reasons above, and providing additional limitations thereto. Reconsideration and withdrawal of the present rejection of these claims are respectfully requested.

Allowable Subject Matter

Applicant gratefully acknowledges the indication of allowability of subject matter in claims 4-6, 13-15, and 23-24. However, the Office Action indicates that the Section 112, 2nd paragraph rejections of claims 4-6 and 13-15 must be overcome, yet there are no such rejections contained in the Office Action of 7/28/2005. Clarification is requested.

Otherwise, the Applicant has opted not to place these claims in independent form because it is entitled to the scope of the independent claims from which they depend, for reasons explained above.

Reasons for Allowability

Applicant acknowledges Examiner's comments (Office Action of 7/28/2005, pg. 8), and has filed herewith a Statement on Examiner's Reasons for Allowable Subject Matter.

Conclusion

This is a complete response to the Office Action mailed July 28, 2005.

Applicant has also filed herewith a Request for Telephone Interview to be held before the Examiner makes the next action on the merits. The interview is necessary to resolve any remaining issues involving the Examiner's Section 112 rejections and rejections over Staszewski '693, wherein Applicant has previously rebutted rejections but Examiner has maintained them without effectively traversing Applicant's rebuttal.

Should any questions arise concerning this response, the Examiner is encouraged to contact the below listed Attorneys.

Respectfully submitted,

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